

System Introduction

1.1 Overview

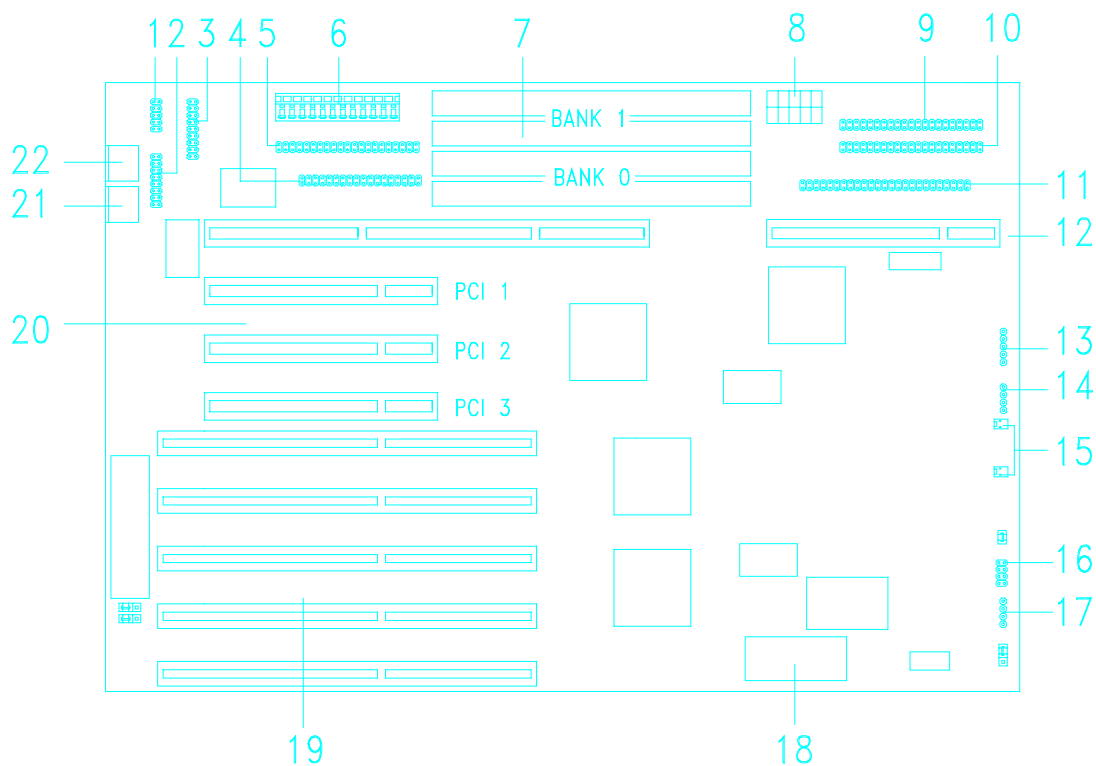
This high-performance system board supports both the 486-series microprocessors and the new Intel Pentium™ microprocessors. The system board does not contain the CPU and the second-level cache. Instead, it has a special slot designed to accommodate a separate board that carries both the CPU and the second-level cache.

Standard features such as two serial ports, one parallel port, diskette drive interface, and embedded fixed disk drive interface reside on the system board, as well as advanced features like the 128-KB system ROM, five 32-bit EISA expansion slots, three PCI local bus slots, four 72-pin SIMM sockets, two enhanced IDE interfaces, and one SCSI interface.

The system board has a 4/8/16-MB base memory and supports a maximum memory of 128 MB using 32-MB single-density SIMMs. When you install the dual Pentium (3.3V) CPU board, you get four additional SIMM sockets and you can use 64-MB SIMMs. With the dual Pentium (3.3V) CPU board, you can have a total system memory of 512 MB using 64-MB SIMMs.

The system board features the single-chip upgrade technology that makes CPU upgrades easy and economical, and the multiple CPU upgrade technology that can convert the system into a multiprocessor system.

1.2 System Board Layout



- | | |
|------------------------------------|--------------------------------|
| 1 COM 2 | 12 CPU board slot |
| 2 COM 1 | 13 Power LED connector |
| 3 Parallel port interface | 14 Hard disk LED connector |
| 4 Diskette drive interface | 15 Fan connectors |
| 5 Fixed disk drive interface | 16 Turbo/Reset connector (J23) |
| 6 Power connector 1 (200/350-watt) | 17 Speaker connector (J24) |
| 7 SIMM sockets | 18 BIOS |
| 8 Power connector 2 (350-watt) | 19 EISA expansion slots |
| 9 Enhanced IDE 1 | 20 PCI slots |
| 10 Enhanced IDE 2 | 21 PS/2 mouse connector |
| 11 Fast SCSI-2 interface | 22 PS/2 keyboard connector |

Figure 1-1 System Board Layout

1.3 Model Definition

Brand Name : Acer
Product Name : AcerAltos 9000
Description : 486/Pentium computer system
Model No. : FXXXHA
Stock No. : F X XX X X - X X X

F X XX X X - X X X

0 : 200W SPS (230V)
1 : 350W SPS (Delta)
2 : 350W SPS (Delta) + Backplane

0 : With SCSI & VGA (ISA), without Fast IDE
1 : With SCSI, without VGA (ISA) & Fast IDE
2 : Without SCSI, with VGA (ISA) & Fast IDE
3 : Without SCSI & VGA (ISA), with Fast IDE

0 : 4MB RAM, 3.5-inch FDD, 256KB cache
1 : 8MB RAM, 3.5-inch FDD, 256KB cache
2 : 16MB RAM, 3.5-inch FDD, 256KB cache, CPU * 1
3 : 16MB RAM, 3.5-inch FDD, 256KB cache, CPU * 2

B : M5 single CPU board
C : M5 dual CPU board

T : IDU
W : ID3P
M : IDT
H : IDAB

33 : 33MHz
50 : 50MHz
60 : 60MHz
66 : 66MHz
75 : 75MHz
90 : 90MHz
00 : 100MHz

Z : 486SX
4 : 486DX
T : 486DX2
5 : Pentium

1.4 System Specifications

1.4.1 System Board Specifications

Table 1-1 System Board Specifications

Item	Specification
Memory	When using the IntelDX4, Pentium (5V), and single Pentium (3.3V) CPU boards: supports 4/8/16/32 MB SIMMs memory expandable to a maximum of 128 MB When using the dual Pentium (3.3V) CPU board: supports 4/8/16/32/64 MB SIMMs memory expandable to a maximum of 512 MB (256 MB on the system board, 256 MB on the dual Pentium 3.3V CPU board)
ROM	128-KB Flash ROM
Real-Time Clock	System clock/calendar that lasts for 5-7 years
Serial Port	One 25-pin, one 9-pin D-type male
Parallel Port	One Centronics standard, 25-pin D-type female
FDD Interface	5.25-inch 1.2-MB and 3.5-inch 1.44-MB diskette drives
HDD Interface	IDE and Enhanced IDE HDD interface
SCSI Interface	Fast SCSI-2
Slots	Five EISA slots Three PCI bus slots One CPU board slot
Power Supply	200/350-watt switching power supply
Keyboard Interface	PS/2-compatible keyboard
Mouse Interface	PS/2-compatible mouse
Operating System	MS-DOS 6.2

1.4.2 Memory Map

Table 1-2 System Memory Map

Address	Size	Function
0000000 ~ 09FFFFh	640 KB	Main memory
0A0000h ~ 0BFFFFh	128 KB	PCI/ISA video buffer memory
0C0000h ~ 0C7FFFh	32 KB	Video BIOS memory
0C8000h ~ 0DFFFFh	96 KB	EISA/ISA card BIOS and buffer memory
0E0000h ~ 0EFFFFh	64 KB	BIOS extension memory Setup and post memory PCI development BIOS memory
0F0000h ~ 0FFFFFFh	64 KB	System BIOS memory
100000h ~ UPPER LIMIT ²		Main memory
UPPER LIMIT ² ~ 4 GB		PCI memory

1.4.3 I/O Address Map

Table 1-3 System I/O Address Map

Address Range (hex)	Device
000 ~ 00F	DMA controller-1
020 ~ 021	Interrupt controller-1
022	ESC configuration address index register
023	ESC configuration data index register
040 ~ 043	System timer 1
048 ~ 04B	System timer 2
060 & 064	Keyboard controller
061	NMI status and control
070	CMOS RAM address and NMI mask
071	CMOS RAM data
080 ~ 08F	DMA page register
0A0 ~ 0A1	Interrupt controller-2
0C0 ~ 0DF	DMA controller-2
0F0	Reset IRQ13
15C ~ 15D	NS87332 base address
1F0 ~ 1F7	Fixed disk
278 ~ 27F	Parallel printer port 3
2F8 ~ 2FF	Serial port 2

Table 1-3 System I/O Address Map (continued)

Address Range (hex)	Device
378 ~ 37F	Parallel printer port 2
3BC ~ 3BE	Parallel printer port 1
3F0 ~ 3F7	Floppy drive controller
3F8 ~ 3FF	Serial port 1
4F0	System port
800 ~ 8FF	EISA NVRAM
C00	EISA NVRAM page register
C80 ~ C83	EISA system board ID
CF8	Configuration space enable register
CF9	Turbo-reset control register
C000 ~ C0FF	PCMC/CDC configuration space
C600 ~ C6FF	PCEB configuration space
C700 ~ C7FF	PCI slot 1
C800 ~ C8FF	PCI slot 2
C900 ~ C9FF	PCI slot 3
CA00 ~ CAFF	Onboard SCSI configuration space
CB00 ~ CBFF	Onboard EIDE configuration space

1.4.4 DMA Channels

Table 1-4 DMA Channels

Channel	Function
0	Available
1	Available / ECP
2	Diskette controller
3	Available / ECP
4	Cascaded
5	Available
6	Available
7	Available

1.4.5 Interrupt Channels

Table 1-5 Interrupt Channels

Channel	Function
IRQ0	Interval timer, counter 0 output
IRQ1	Keyboard
IRQ2	Cascaded interrupt
IRQ3	COM2 / PCI slot
IRQ4	COM1 / PCI slot
IRQ5	Printer / PCI slot
IRQ6	Floppy controller
IRQ7	Printer / PCI slot
IRQ8	Real-time clock
IRQ9	Reserved / PCI slot
IRQ10	Reserved / PCI slot
IRQ11	Reserved / PCI slot
IRQ12	Mouse
IRQ13	NPX error
IRQ14	ISA IDE / PCI EIDE
IRQ15	ISA IDE / PCI EIDE

1.4.6 Cache Configuration

Table 1-6 Pentium (5V) and Single Pentium (3.3V) Cache Configuration

Size	256KB
Data RAM	32KB x 8, 15ns, 5V
TAG / Dirty / Valid	Internal to PCMC
Cacheable memory	256 MB

Table 1-7 IntelDX4 Cache Configuration

Size	256KB
Data RAM	32KB x 8, 15ns, 5V
TAGs / Dirty / Valid	32KB x 3, 15ns, 5V
Cacheable memory	128 MB

Table 1-8 Dual Pentium (3.3V) Cache Configuration

Size	256KB
Data RAM	32KB x 8, 15ns, 3.3V
TAGs / Dirty / Valid	Internal to PCMC
Cacheable memory	512 MB

Dual Pentium (3.3V) Cache Upgrade

When using the dual Pentium (3.3V) CPU board, you can upgrade the second-level cache as follows:

- Upgrade to 512 KB by plugging in a 256-KB cache board
- Upgrade to 512 KB by plugging in a 512-KB synchronous-type cache board

1.4.7 Special I/O Port Definition

A special I/O port is for decoding specific functions as defined by the system designer. The address of the special I/O port is chosen such that it does not conflict with the other system ports.

1.4.8 Memory Type and Memory Upgrade Path

The system comes with a standard 4/8/16-MB memory, expandable to 128 MB or 256 MB depending on the type of CPU board installed. You can upgrade the system memory by adding single inline memory modules (SIMMs) into the SIMM sockets or by changing the SIMMs for a higher memory configuration. The four 72-pin SIMM sockets support 4-MB and 16-MB single-density as well as 8-MB and 32-MB double-density SIMMs. When available, you may also plug-in 64-MB single-density SIMMs, if a dual-Pentium (3.3V) CPU board is installed.

Table 1-9 lists the available memory configurations when the system uses either an IntelDX4, Pentium (5V), or single Pentium (3.3V) CPU board.

Table 1-9 Memory Configurations*

Bank 0		Bank 1		Total Memory
Socket 0	Socket 1	Socket 0	Socket 1	
4 MB	4 MB			8 MB
4 MB	4 MB	4 MB	4 MB	16 MB
8 MB	8 MB			16 MB
8 MB	8 MB	4 MB	4 MB	24 MB
4 MB	4 MB	8 MB	8 MB	24 MB
8 MB	8 MB	8 MB	8 MB	32 MB
16 MB	16 MB			32 MB
16 MB	16 MB	4 MB	4 MB	40 MB
4 MB	4 MB	16 MB	16 MB	40 MB
16 MB	16 MB	8 MB	8 MB	48 MB
8 MB	8 MB	16 MB	16 MB	48 MB
16 MB	16 MB	16 MB	16 MB	64 MB
32 MB	32 MB			64 MB
32 MB	32 MB	4 MB	4 MB	72 MB
4 MB	4 MB	32 MB	32 MB	72 MB
32 MB	32 MB	8 MB	8 MB	80 MB
8 MB	8 MB	32 MB	32 MB	80 MB
32 MB	32 MB	16 MB	16 MB	96 MB
16 MB	16 MB	32 MB	32 MB	96 MB
32 MB	32 MB	32 MB	32 MB	128 MB

On models using the dual-Pentium (3.3V) CPU board, four additional 72-pin SIMM sockets are available. With the additional sockets, you can upgrade the memory to 512 MB using 64-MB SIMMs.

Table 1-10 lists some of the possible memory configurations when a dual-Pentium (3.3V) CPU board is installed.

NOTE: Banks 0 and 1 are on the system board; banks 2 and 3 are on the dual Pentium CPU board.

* When using the IntelDX4, Pentium (5V), and single Pentium (3.3V) CPU boards

Table 1-10 Some Possible Memory Configurations When Using the Dual Pentium (3.3V) CPU Board

Bank 0		Bank 1		Bank 2		Bank 3		Total Memory
Socket 0	Socket 1	Socket 0	Socket 1	Socket 0	Socket 1	Socket 0	Socket 1	
4 MB	4 MB	4 MB	4 MB					16 MB
4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	32 MB
8 MB	8 MB	8 MB	8 MB	4 MB	4 MB	4 MB	4 MB	48 MB
16 MB	16 MB	8 MB	8 MB	4 MB	4 MB	4 MB	4 MB	64 MB
16 MB	16 MB	16 MB	16 MB	16 MB	16 MB	16 MB	16 MB	128 MB
32 MB	32 MB	32 MB	32 MB	16 MB	16 MB	16 MB	16 MB	192 MB
32 MB	32 MB	32 MB	32 MB	32 MB	32 MB	32 MB	32 MB	256 MB
64 MB	64 MB	64 MB	64 MB					256 MB
64 MB	64 MB	64 MB	64 MB	64 MB	64 MB	64 MB	64 MB	512 MB

Take note of the following when adding memory:

- Always install SIMMs from the lowest bank first. For example, install SIMMs in bank 0 before bank 1, bank 1 before bank 2, and so on.
- Always remove SIMMs from the highest bank first. For example, bank 3 before bank 2, and so on.
- Use only the same type of SIMM in a given bank.
- You may combine different types of SIMMs for a particular memory configuration as long as the SIMMs in each bank are of the same type.

IMPORTANT: *You must disable the BIOS parameter System Parity if you installed SIMMs without parity.*

1.5 CPU Boards

The system main board has one CPU slot that supports the following CPU boards:

- IntelDX4™ CPU board
- Intel Pentium™ processor CPU board (5V)
- Intel Pentium™ Processor CPU board (3.3V) - single
- Intel Pentium™ Processor CPU board (3.3V) - dual

The following sections give detailed information on each CPU board.

NOTE: *For simplicity, the three Pentium CPU boards will be referred to as **Pentium (5V)**, **single Pentium (3.3V)**, and **dual Pentium (3.3V)**, respectively, throughout this manual.*

1.5.1 IntelDX4

The IntelDX4 CPU board supports the following CPU types:

- 486DX/33
- 486DX2/50
- 486DX2/66
- IntelDX4 (P24C)/100 MHz

The CPU board supports both 3.3V and 5V CPUs. It has an auto-sensing voltage regulator that supplies the 3.3V power to low-voltage CPU. The 256-KB second-level cache and the Saturn II chipset that includes one CDC and one DPU also reside on the board.

1.5.2 Pentium (5V)

The Pentium (5V) CPU board supports the Intel Pentium CPU running at either 60 or 66 MHz with an operating voltage of 5V, a Mercury chipset that includes one PCMC and two LBXs, and 256-KB second-level cache.

1.5.3 Single Pentium (3.3V)

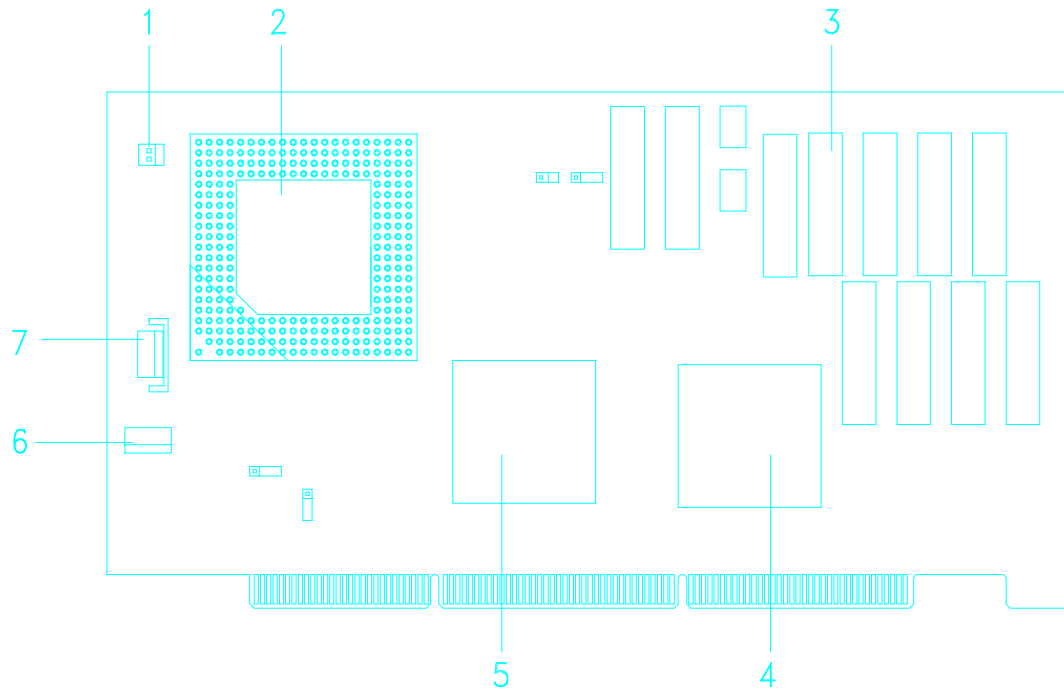
The single Pentium (3.3V) CPU board consists of an Intel Pentium Processor running at either 90 or 100 MHz in its ZIF 320-pin upgrade socket, a Mercury chipset that includes one PCMC and two LBXs, and a 256-KB second-level cache.

1.5.4 Dual Pentium (3.3V)

The dual Pentium (3.3V) CPU board carries two Intel Pentium Processors in its 296-pin LIF and 320-pin ZIF sockets, 256-KB second-level cache, four 72-pin SIMM sockets, a Neptune chipset that consists of one PCMC and two LBXs.

.6 CPU Board Layouts

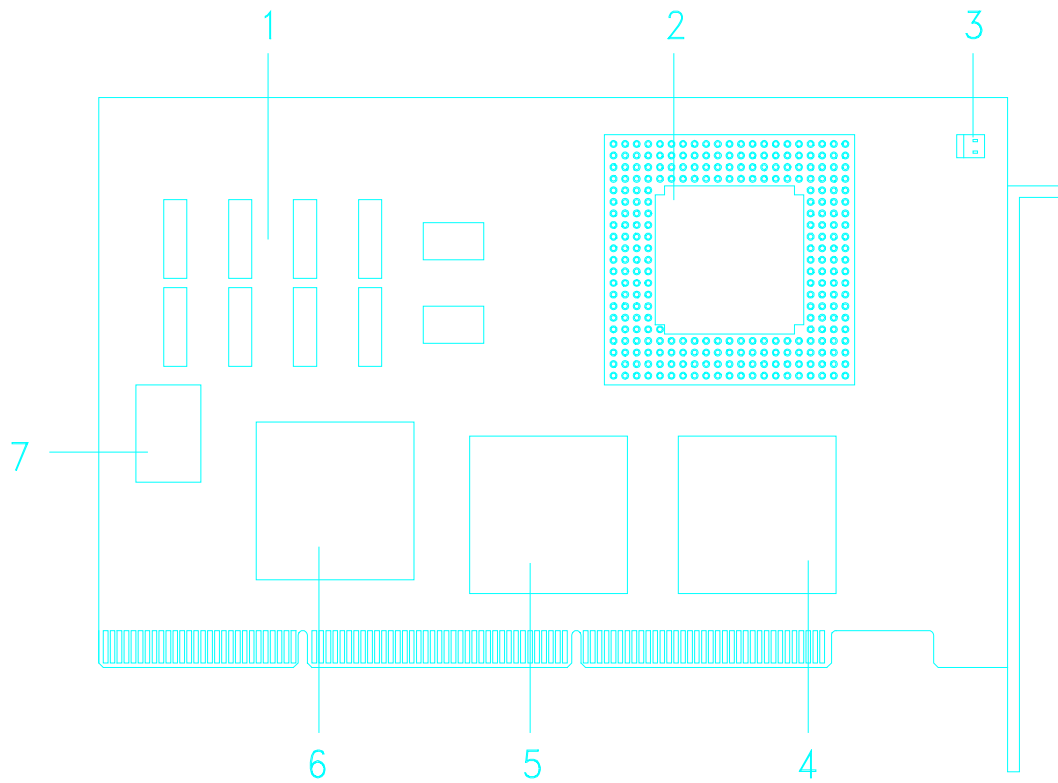
1.6.1 IntelDX4



- | | |
|----------------------|---------------------|
| 1 Fan connector | 5 Saturn CDC |
| 2 CPU socket | 6 5V switch |
| 3 Second-level cache | 7 Voltage regulator |
| 4 Saturn DPU | |

Figure 1-2 IntelDX4 CPU Board Layout

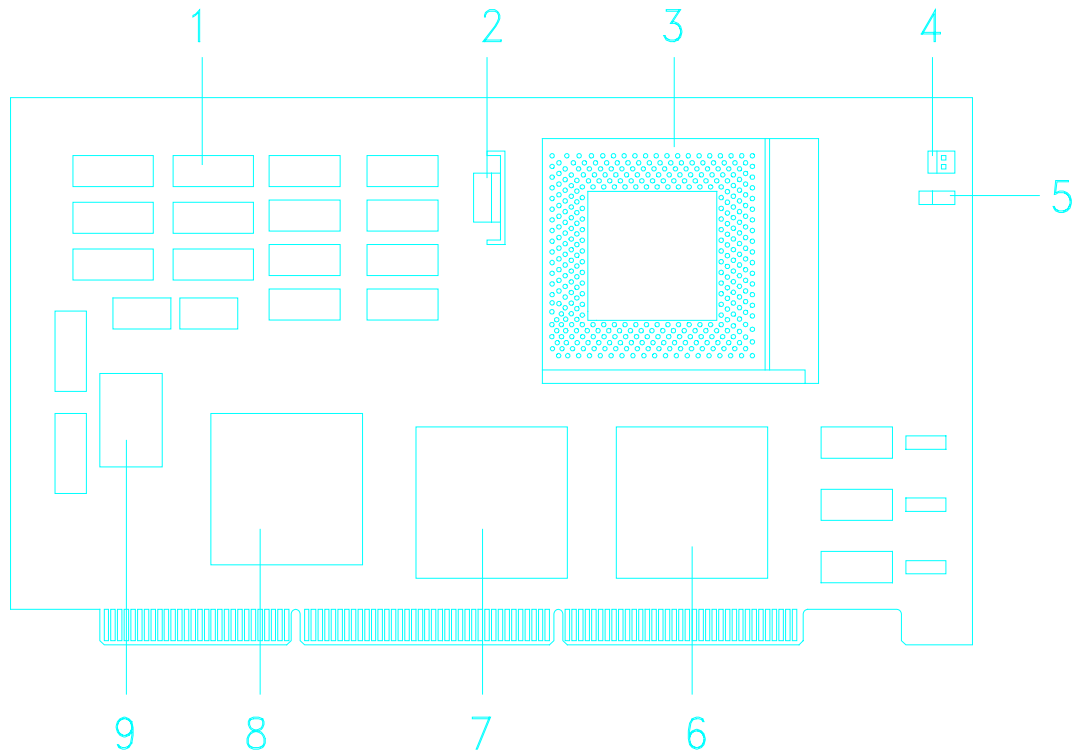
1.6.2 Pentium (5V)



- | | |
|----------------------|--------------|
| 1 Second-level cache | 5 LBX |
| 2 CPU socket | 6 PCMC |
| 3 Fan connector | 7 Oscillator |
| 4 LBX | |

Figure 1-3 Pentium (5V) CPU Board Layout

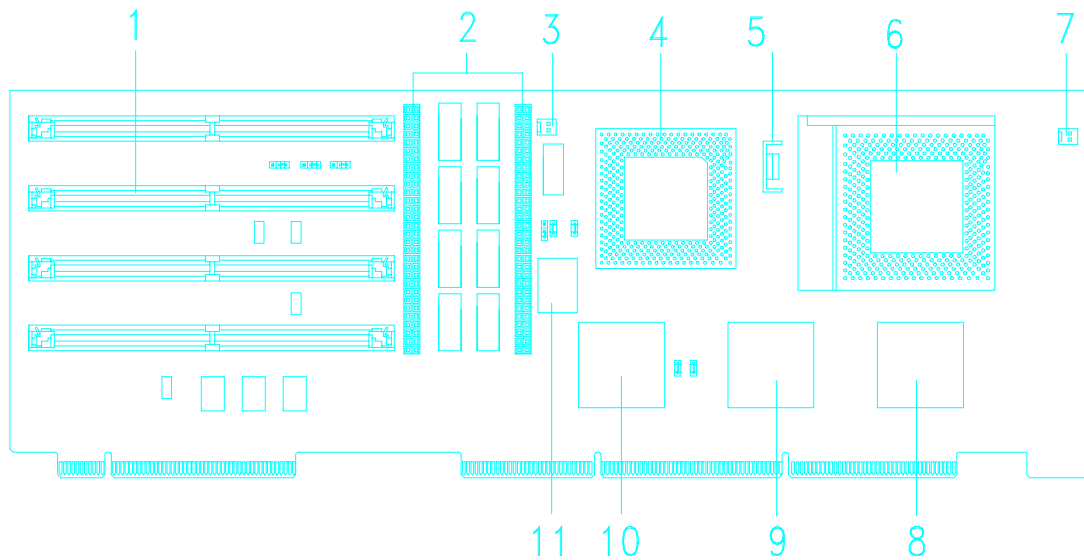
1.6.3 Single Pentium (3.3V)



- | | |
|----------------------|--------------|
| 1 Second-level cache | 6 LBX |
| 2 Voltage regulator | 7 LBX |
| 3 CPU socket | 8 PCMC |
| 4 Fan connector | 9 Oscillator |
| 5 JP1 | |

Figure 1-4 Single Pentium (3.3V) CPU Board Layout

1.6.4 Dual Pentium (3.3V)



- | | | | |
|---|------------------------------------|----|---------------|
| 1 | SIMM sockets | 7 | Fan connector |
| 2 | Second-level cache board connector | 8 | LBX |
| 3 | Fan connector | 9 | LBX |
| 4 | Pentium (3.3V) CPU LIF-type socket | 10 | PCMC |
| 5 | Voltage regulator | 11 | Oscillator |
| 6 | Pentium (3.3V) CPU ZIF-type socket | | |

Figure 1-5 Dual Pentium (3.3V) CPU Board Layout

1.7 Block Diagrams

1.7.1 System Block Diagram – IntelDX4 CPU

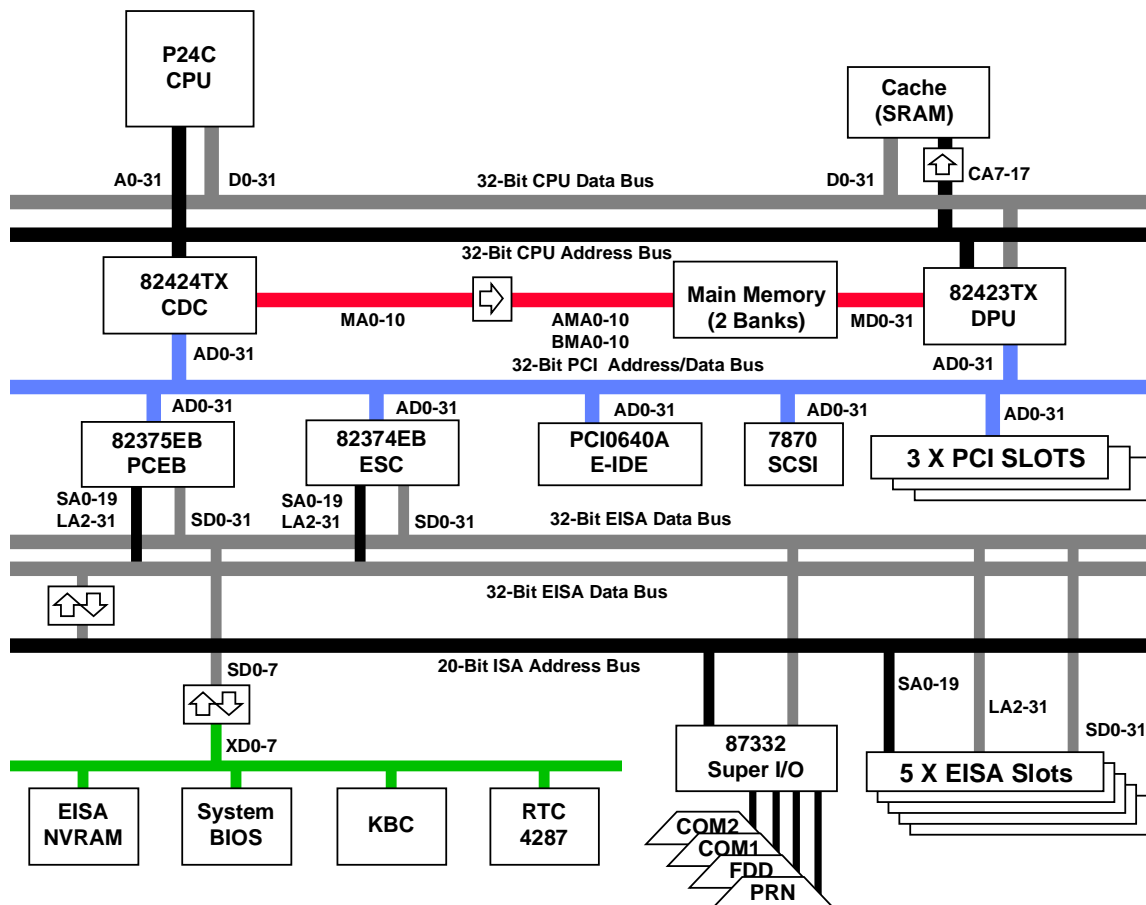


Figure 1-6 System Block Diagram – IntelDX4 CPU

1.7.2 System Block Diagram – Pentium (5V) CPU

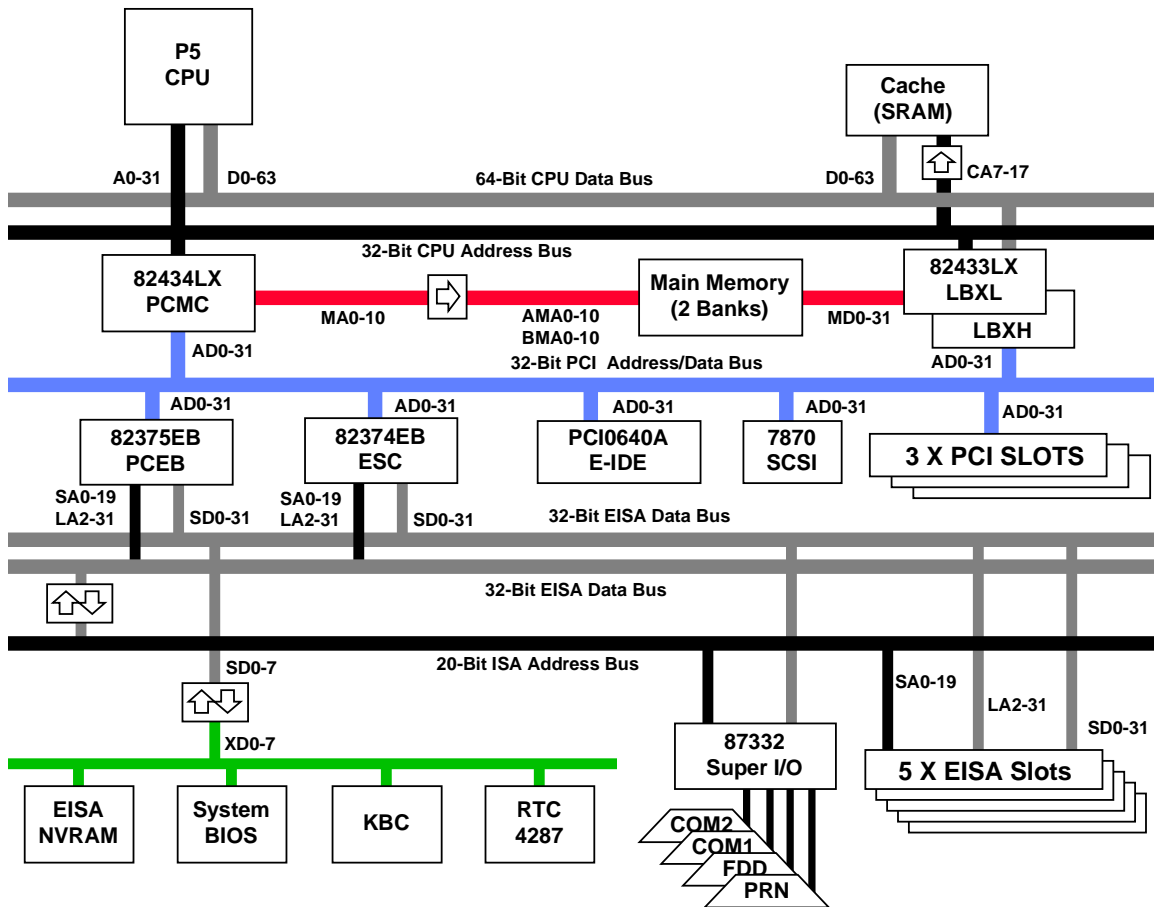


Figure 1-7 System Block Diagram – Pentium (5V) CPU

1.7.3 System Block Diagram – Single Pentium (3.3V) CPU

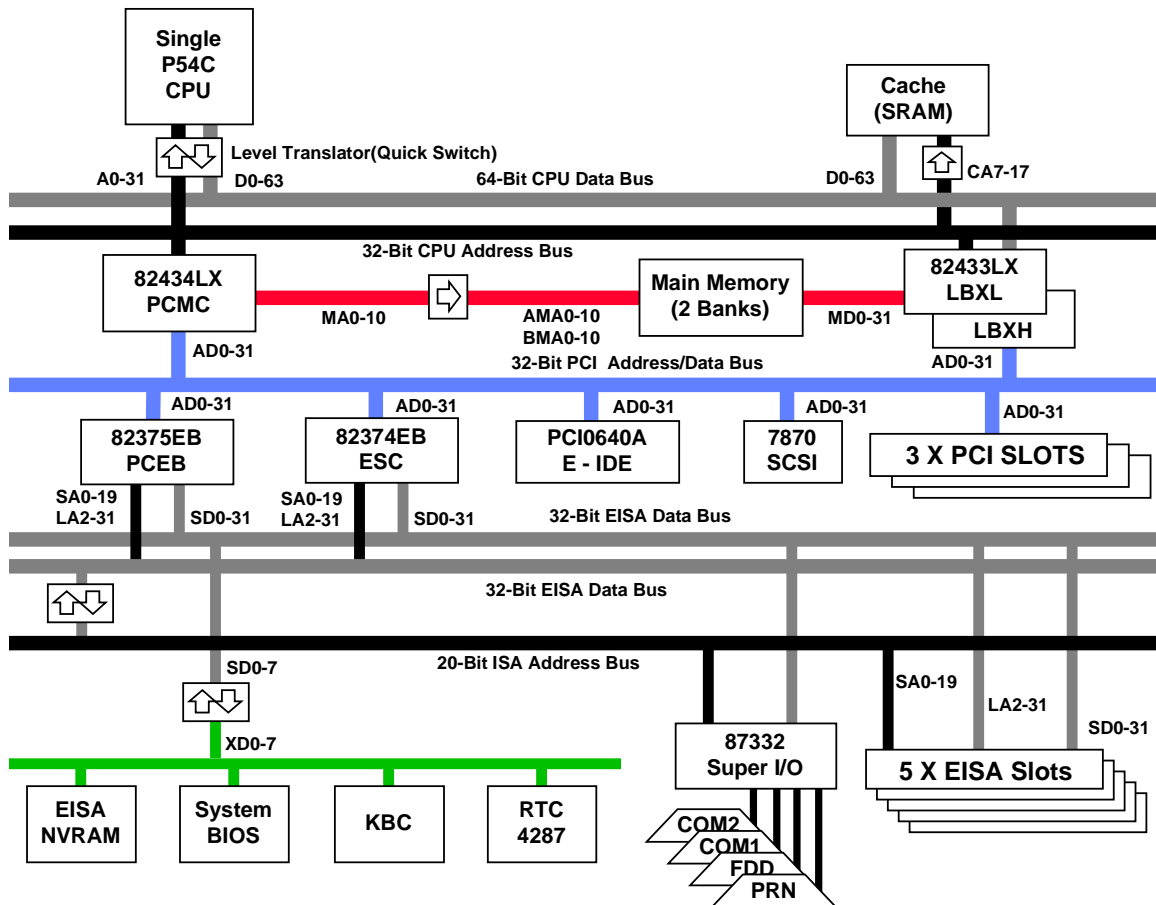


Figure 1-8 System Block Diagram – Single Pentium (3.3V) CPU

1.7.4 System Block Diagram – Dual Pentium (3.3V) CPU

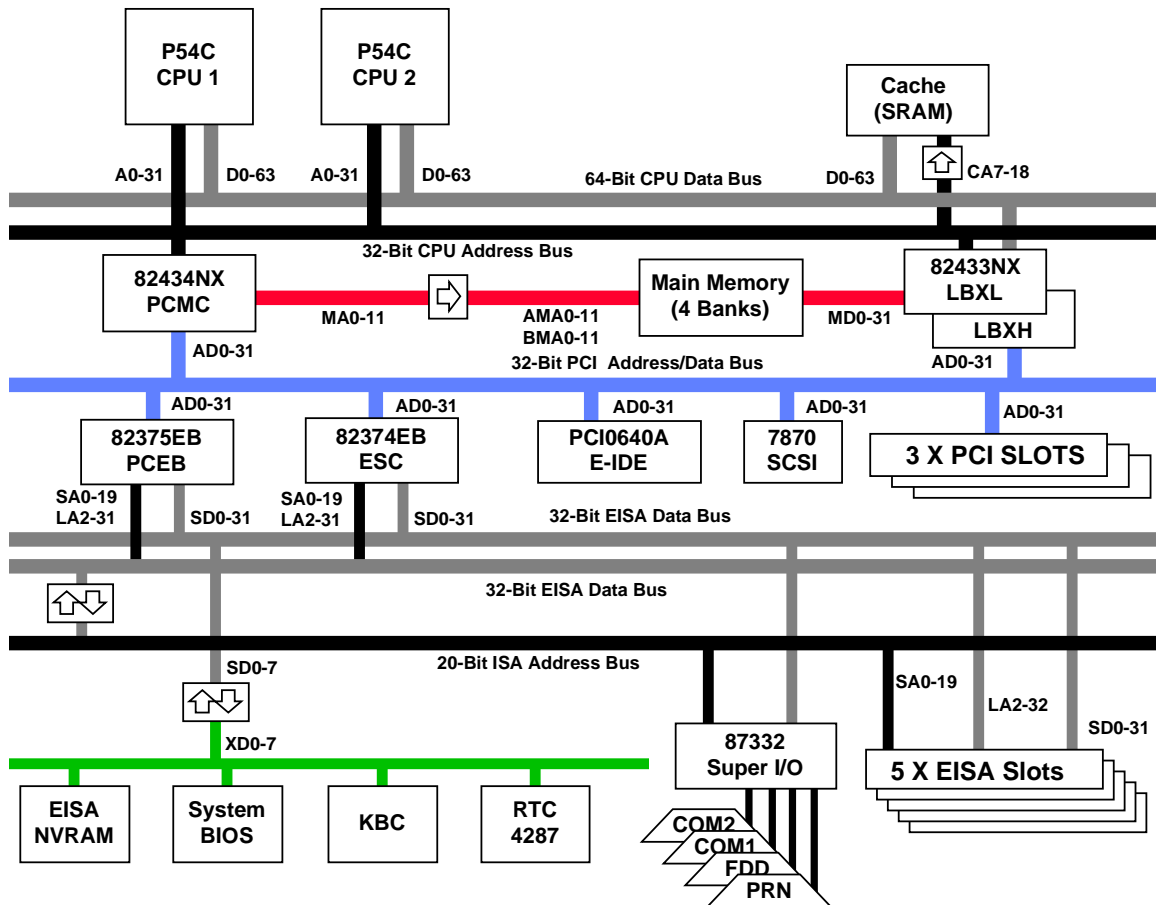


Figure 1-9 System Block Diagram – Dual Pentium (3.3V) CPU

1.8 System Description

1.8.1 System Bus Diagram

The 82434LX PCI/Cache/Memory Controller (PCMC) supports a memory address and memory refresh control interface to the DRAM, cache interface, and the PCI control signal interface.

There are two 82433LX local-bus accelerators (LBX) which are controlled by PCMC. The LBXs internally decode the signals from PCMC to offer a 64-bit memory data interface to the DRAM and a 32-bit address/data interface to the PCI socket. Each LBX has five integrated write posting and read prefetch buffers for increasing the performance.

The 82374EB EISA System Component (ESC) and 82375EB PCI-EISA Bridge (PCEB) together provide the EISA system compatible master/slave functions on both the PCI local bus and the EISA bus and the common I/O functions found in current EISA systems. The ESC incorporates the logic for an EISA (master and slave) interface, EISA bus controller, enhanced seven-channel DMA controller with Scatter-Gather support, EISA arbitration, 14-channel interrupt controller, five programmable timer/counters and non-maskable control logic. The ESC also integrates support logic to decode peripheral devices such as the Flash BIOS, real-time clock, keyboard/mouse controller, diskette drive controller, two serial ports, one parallel port, and IDE hard disk drive. The PCEB provides the address and data paths, bus controls, and bus protocol translation for PCI-to-EISA and EISA-to-PCI transfers. Extensive data buffering in both directions increase system performance by maximizing PCI and EISA bus efficiency and allowing concurrency on the two buses. The PCEB integrates central bus control functions, PCI parity generation, system error reporting, and programmable PCI and EISA memory and I/O address space mapping and decoding.

1.8.2 LBX: Data Buffers

The LBX has five write posting and read prefetch buffers. These increase the CPU and PCI master performance by:

1. CPU-to-memory posted write buffer: 4 quadwords deep.
It enables the Pentium processor to write-back a whole cache line at the fastest speed.
2. PCI-to-memory posted write buffer: 2 buffers, each is 4 dwords deep.
A PCI master can post two consecutive sets of 4 dwords (total of one cache line) or two single non-consecutive transactions.
3. PCI-to-memory read prefetch buffer: 4 quadwords deep.
A PCI master-to-memory read transaction causes this prefetch buffer to read up to 4 quadwords of data from memory, allowing up to 8 dwords to be read onto PCI in a single burst transaction.
4. CPU-to-PCI posted write buffer: 4 dwords deep.
Pentium can post up to 4 dwords into this buffer.
5. CPU-to-PCI read prefetch buffer: 4 dwords deep.
It enables faster Pentium sequential reads when targeting PCI.

With the exception of the PCI-to-memory write buffer and CPU-to-PCI write buffer, the buffers in the LBX store data only, address are stored in the PCMC.

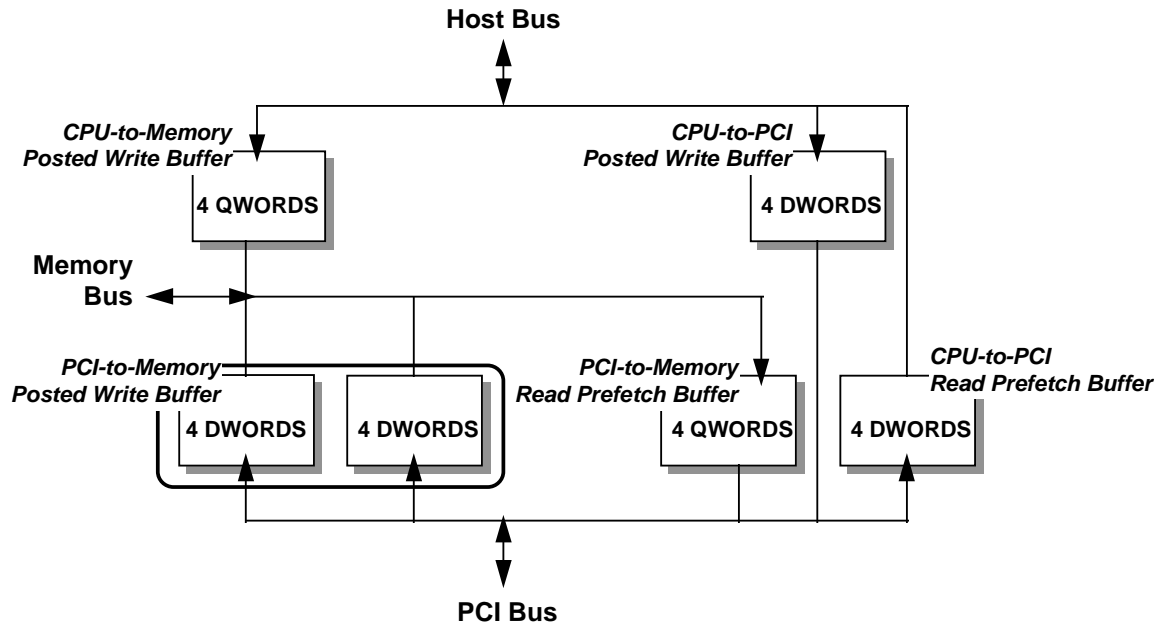


Figure 1-10 LBX: Data Buffers Block Diagram

1.8.3 LBX: System Bus Interconnect

Since the PCI connection for each LBX falls on 16-bit boundaries, each does not simply connect to either the low dword or high dword of the quadword memory and host buses. Instead, the low order LBX buffers connect to the first and third words of each 64-bit bus while the high order LBX buffers connect to the second and fourth words of the memory and host buses.

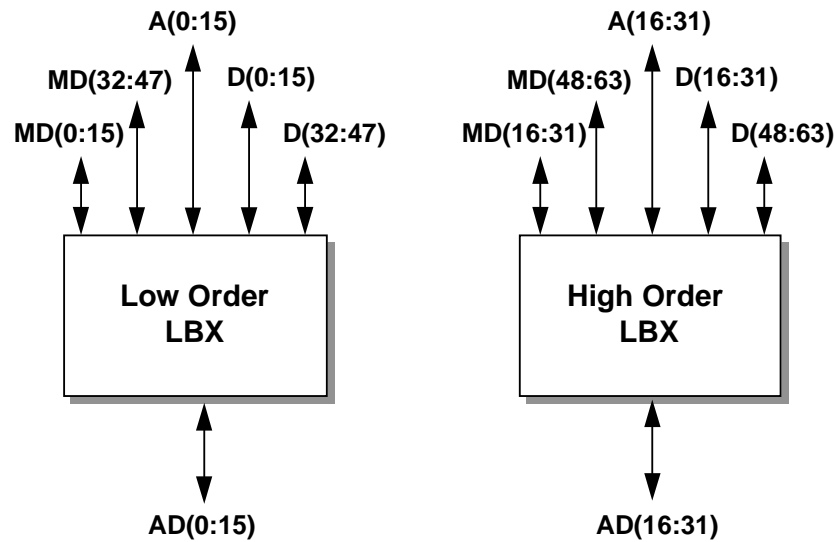


Figure 1-11 LBX: System Bus Interconnect Block Diagram

1.8.4 Host Clock Path

The PCMC and LBXs operations are based on two clocks, HCLK and PCLK.

- The CPU, second-level cache, and the DRAM interface operations are based on HCLK.
- The PCI interface timing is based on PCLK.

The clock originates from the oscillator which is connected to the HCLKOSC of PCMC. The PCMC generates six copies of HCLK, HCLKA~HCLKF.

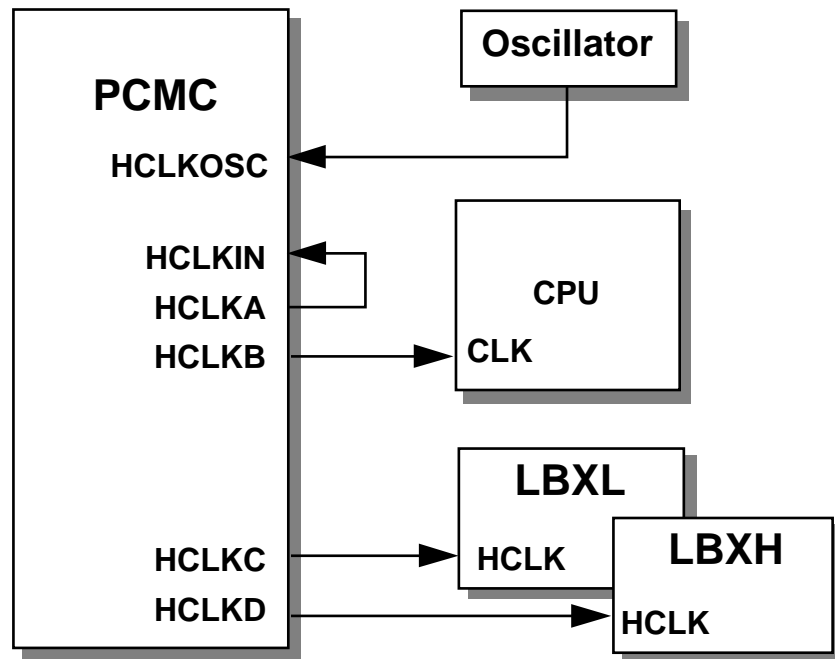


Figure 1-12 Host Clock Path Block Diagram

1.8.5 PCI Clock Path

The PCMC drives the PCLKOUT to an external clock driver which supplies copies of PCLK to PCI devices, LBXs, and back to the PCMC.

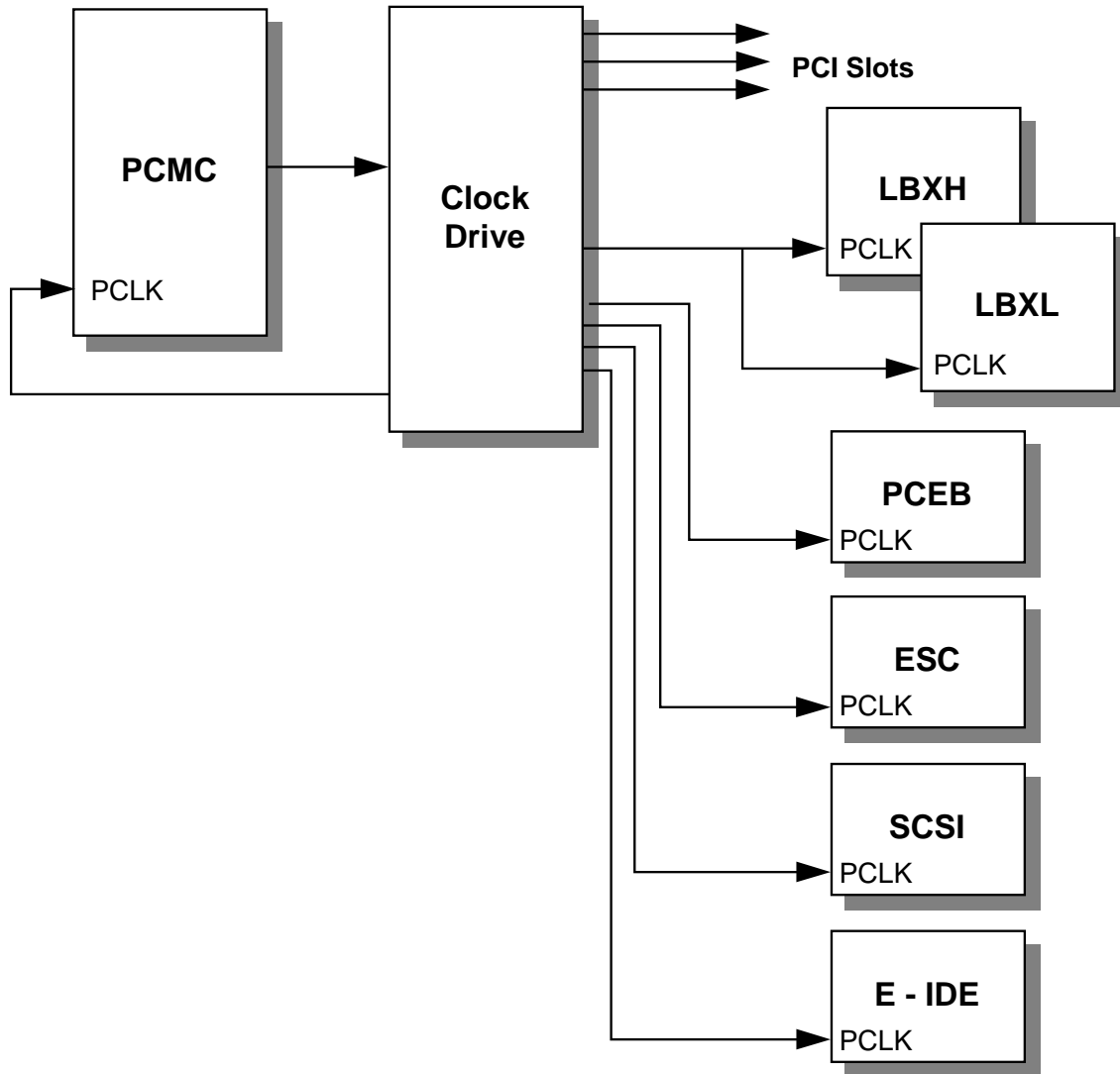


Figure 1-13 PCI Clock Path Block Diagram

1.8.6 Cache Management

The PCMC supports integrated tags, and full first-level and second-level cache coherency mechanisms.

The PCMC contains 4096 address tags, each tag representing a sector in the second-level cache. Upon a CPU read cache miss, the PCMC inspects the valid and modified bits within the addressed sector and writes back to main memory only the lines marked both valid and modified. All lines in the sector are then invalidated. The line fill occurs and the valid bit associated with the allocated line is set. Only the requested line is fetched from main memory and written into the cache. If no write is marked invalid, the line fill then occurs and the valid bit associated with the allocated line is set. Lines are not allocated on writes are missed. When a CPU write hits a line in the second-level cache, the modified bit for the line is set.

When CALE is asserted, HA[17:7] flow through the address latch. When CALE is negated, the address is captured in the latch, allowing the processor to pipeline the next bus cycle onto the address bus.

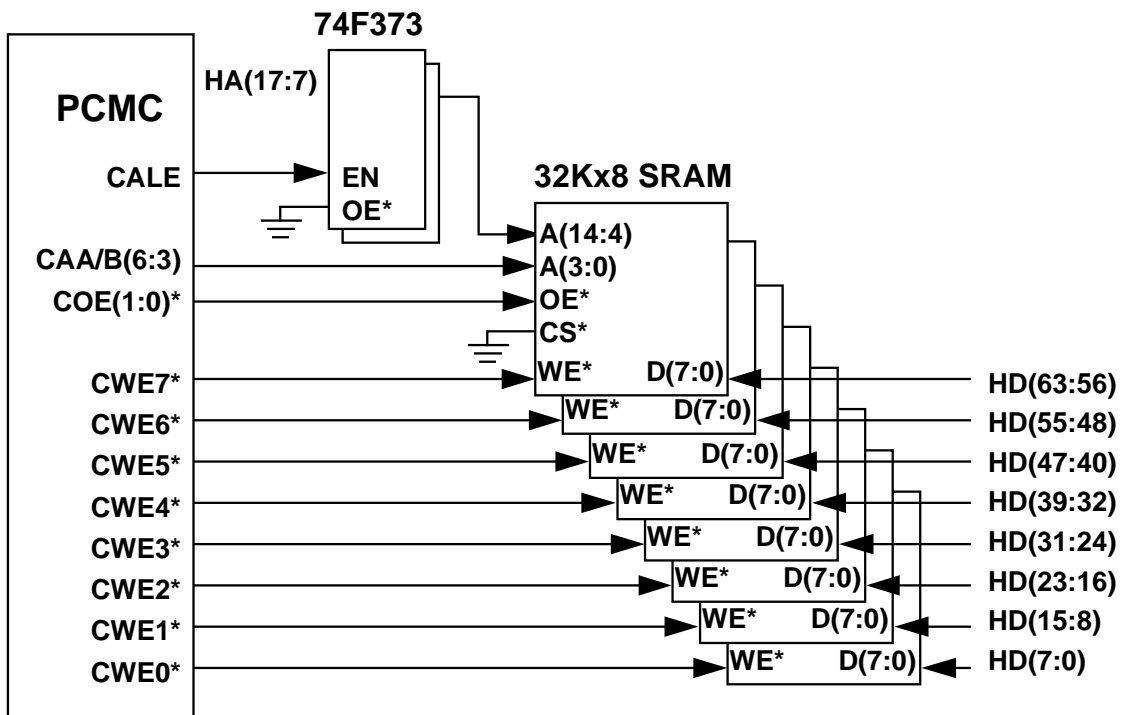


Figure 1-14 Cache Management Block Diagram

1.8.7 Memory Management

The PCMC controls a 64-bit memory array ranging from 2 MB up to 128 MB using the industry standard single- or double-density 36-bit memory modules with fast page-mode DRAMs. The eleven multiplexed address lines MA[10:0] allow the PCMC to support 256K x 36, 1M x 36, 4M x 36 and 8M x 36 SIMMs. The PCMC has six RAS* lines that support up to six rows of DRAM. Eight CAS* lines allow byte control over the array during read and write operations. The PCMC DRAM interface is synchronous to the CPU clock and supports page mode access to efficiently transfer data in bursts of four quadwords.

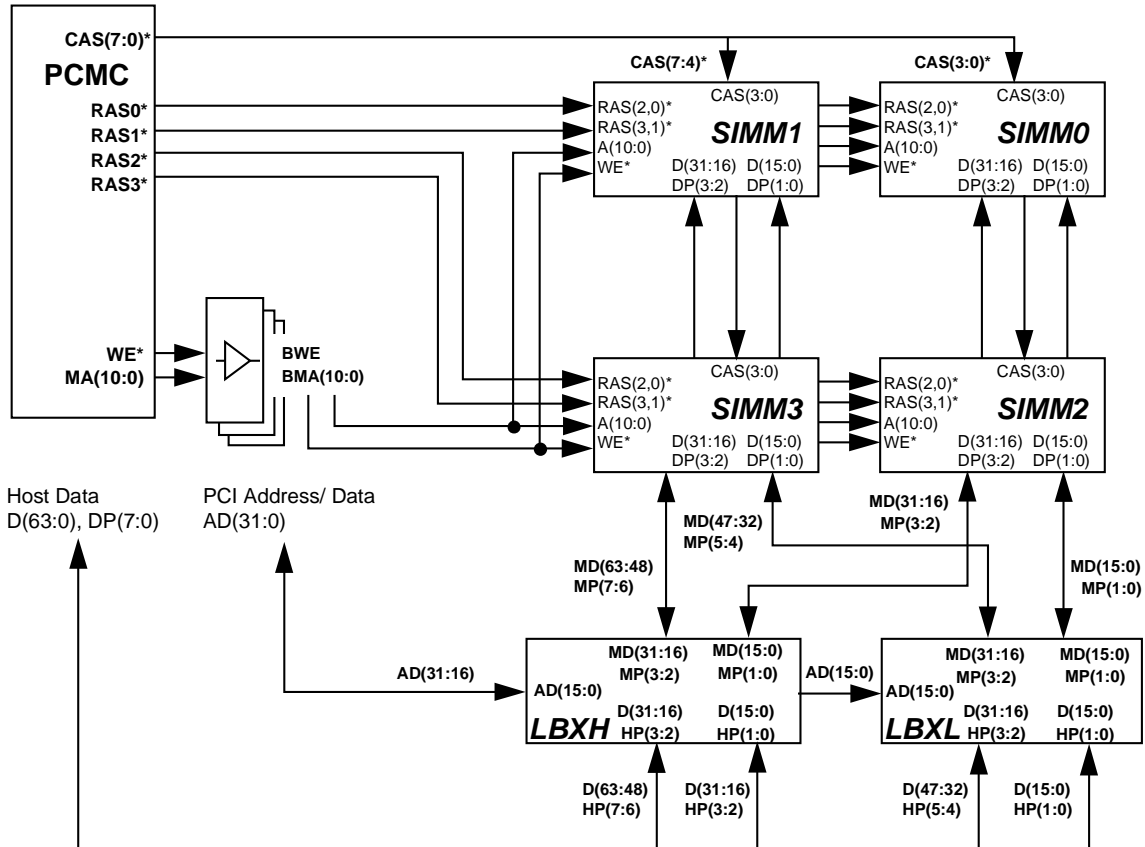


Figure 1-15 Memory Management Block Diagram
(with IntelDX4, Pentium 5V and Single Pentium 3.3V CPU Boards)

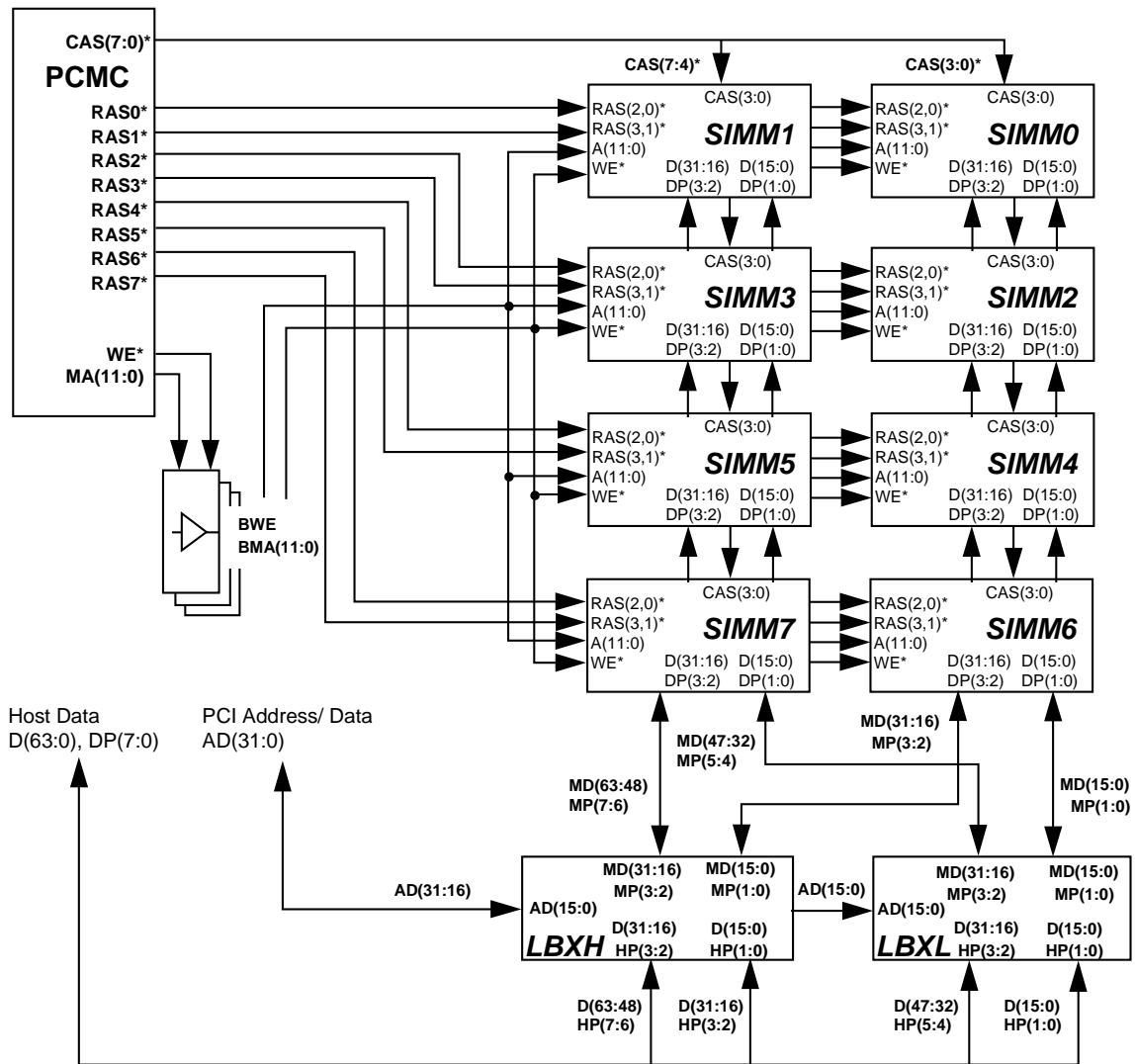


Figure 1-16 Memory Management Block Diagram (with Dual Pentium 3.3V CPU Board)

1.9 BIOS Setup

The following sections give you the technical descriptions of several unique parameters found in BIOS version V2.0R02-A0. Refer to the User's Manual for more information regarding System Configuration.

1.9.1 Basic System Configuration

Basic System Configuration		Page 2/2
Communication Settings		
Baud Rate -----	[9600] BPS	
Parity -----	[Odd]	
Stop Bits -----	[1] Bits	
Data Length -----	[7] Bits	
Enhanced IDE Features		
❶ IDE Fixed Disk Block Mode -----	[Disabled]	
❷ Large Hard Disk Capacity -----	[Disabled]	
Num Lock After Boot -----	[Enabled]	
Memory Test -----	[Disabled]	
❸ Auto Configuration Mode -----	[Enabled]	
❹ Fast Boot Mode -----	[Enabled]	
↑ ↓ = Move Highlight Bar, → ← = Change Setting PgDn/PgUp = Move Screen, F1 = Help, Esc = Exit		

❶ IDE Fixed Disk Block Mode

The conventional HDD accesses one sector (512KB) every I/O read/write operation. Whether the HDD space is continuous or not, a number of I/O read/write commands are performed in the IDE interface if the system wants to access more than one HDD space sector. The execution of these I/O commands requires longer time, thus slowing the data transfer. In Block mode, HDD executes only one I/O read/write command when accessing a continuous space to HDD. This increases the IDE transfer volume. If this parameter is set to *Enabled*, the IDE I/O read/write command is accompanied by an annotation of the beginning and the end sector. After the first sector is transferred completely, the second sector is transferred according to the address of the first sector plus one. Then, the third sector is transferred according to the address of second sector plus one, etc. The cycle continues until the end sector is reached.

If your fixed disk does not support the block mode feature, BIOS automatically bypasses this function even if the parameter is enabled. At present, most IDE HDD support the IDE Block Mode feature.

- ② Large Hard Disk Capacity The HDD capacity is limited at 528MB under the conventional BIOS and the DOS environment. Through the E-IDE interface and some modification of the BIOS settings, this limitation is solved. If your HDD capacity is larger than 528MB, this parameter must be set to Enabled.
- ③ Auto Configuration Mode Set this parameter to Enabled if you do not know the HDD type parameters and the onboard communication port configuration. When enabled, this parameter automatically sets the system speed to High, configures the HDD type, and enables the system and video shadow RAM, internal cache, and external cache.
- ④ Fast Boot Mode This parameter enables the system to boot faster by skipping some Power-On Self-Test (POST) routines such as memory test, system chips initialization, etc.

1.9.2 Advanced System Configuration

Advanced System Configuration		Page 1/1
❶ Shadow RAM		
E0000h - FFFFFh (System BIOS) -----	[Enabled]	
C0000h - C7FFFh (Video BIOS)-----	[Enabled]	
C8000h - CFFFFh -----	[Disabled]	
D0000h - D7FFFh-----	[Disabled]	
D8000h - DFFFFh -----	[Disabled]	
Internal Cache (CPU Cache) -----	[Enabled]	
External Cache -----	[Enabled]	
Cache Scheme -----	[Write Back]	
System Memory Parity -----	[Enabled]	
❷ Memory at 15MB-16MB Reserved for -----	[System]	Use
E0000h - FFFFFh (System BIOS) -----	[Cacheable]	
C0000h - C7FFFh (Video BIOS) -----	[Cacheable]	
↑ ↓ = Move Highlight Bar, → ← = Change Setting PgDn/PgUp = Move Screen, F1 = Help, Esc = Exit		

❶ Shadow RAM

The ROM access time is slower than RAM. To reduce the access time, the system ROM or I/O ROM is mapped as Shadow RAM. When the system accesses ROM, the access is redirected to RAM where the memory area is defined as “Read only”.

Add-on cards may either have the RAM or the ROM with RAM embedded to store the system configuration. If you set the memory area as Shadow RAM, then the memory is defined as “Read only”. As a result, the system configuration information cannot be written to the RAM of the add-on cards as this would cause system collision. In order to avoid errors when installing these kinds of add-on cards, users should not set the memory area to Shadow RAM.

❷ Memory at 15MB-16MB

This parameter must be set to Reserved for System Use if your system is using some out-of-date add-on cards that require the use of this memory area. This function is backward-compatible with current out-of-date products in the market.

1.9.3 PCI System Configuration

PCI System Configuration		Page 1/1
❶	PCI Slot Number ----- [1]	
❷	Function Number of Device ----- [0]	
❸	Device Function ----- [Disabled]	
❹	Bus Master ----- [Disabled]	
❺	IRQ Level for INTA Pin ----- [--]	
	IRQ Level for INTB Pin ----- [--]	
	IRQ Level for INTC Pin ----- [--]	
	IRQ Level for INTD Pin ----- [--]	
	Onboard SCSI AIC-7870 ----- [Disabled]	
	Boot Device ----- [Disabled]	
	IRQ Level for INTA Pin ----- [--]	
❻	VGA Palette Snoop ----- [Disabled]	
↑ ↓ = Move Highlight Bar, → ← = Change Setting PgDn/PgUp = Move Screen, F1 = Help, Esc = Exit		

- ❶ PCI Slot Number This parameter lets you choose the PCI slot to configure based on the succeeding subitems.

- ❷ Function Number of Device You need to identify the function number assigned for each specific function of the PCI cards with multi-function feature. Since multi-function PCI cards are not yet available in the market, this function is reserved for future use.

- ❸ Device Function This setting allows you enable or disable the PCI device. When set to Enabled, the system activates the PCI device upon booting. When set to Disabled, the system boots without activating the device even it is installed in the PCI slot.

- ❹ Bus Master This function must be enabled if the PCI card supports the bus master feature. Bus master issues commands to hold the CPU, to use the local-bus, and to access memory directly.

- ❺ IRQ Level for INTA Pin Each PCI slot has 4 Interrupts (INTA, B, C, D). These INTx must be converted into IRQx. Once converted, the M1435 recognizes and accepts the IRQs. Multi-function PCI cards may use more than one INTx. In this case, you must assign a specific IRQx for each INTx. Make sure that you assign a different IRQx for each INTx.

- ❻ VGA Palette Snoop This setting controls the PCI VGA compatible device access to the palette registers. When this is set to Enabled, special palette snooping behavior is also enabled. When the setting is Disabled, the device treats palette accesses as ordinary accesses.

1.10 Power Requirements

The specific housing configuration of the system determines the total power consumption required by the system. The switching power supply (SPS) supplies 200W for a system with either an ID3P or IDAB housing. The motherboard's power consumption, such as minimum load, maximum load and surge (peak) current should fit the specification of the SPS. The system supports power supply that meets the following specifications:

1.10.1 200W Power Supply Specifications

Input Requirements

- Maximum waveform harmonic distortion shall be less than 5 percent. The power supply must operate above frequency with both 100~120/200~240 VRMS input voltage ranges.
- The power supply must operate over both voltage ranges with an outside switch.

Table 1-11 200W Power Supply Input Requirements

Input Frequency	Nominal Frequency 50 Hz 60 Hz	Frequency Variations 47 Hz ~ 53 Hz 57 Hz ~ 63 Hz
Input Voltage	Nominal Voltage 100 ~ 120 VRMS 200 ~ 240 VRMS	Variation Range 90 ~ 132 VRMS 180 ~ 264 VRMS
Input Current	Maximum Input Current 8.0A 4.0A	Measuring Range 90 ~ 132 VRMS 180 ~ 264 VRMS
Inrush Current	The power supply inrush current shall be less than the ratings of its critical components (including the fuse, rectifiers, and the surge-limiting device) for all conditions of line voltage.	
Efficiency	65% minimum (measuring at max. load, applying nominal line)	

Output Requirements

- Ripple and noise bandwidth from DC to 20 MHz
- +12V should provide 10A surge current for the first 10 seconds after power on, and this regulation should be within +7% and -6%.
- Total power consumption is 200 watts.

Table 1-12 200W Power Supply Output Ratings (measured at output power connector)

Output	Nominal	Regulation	Minimum Output Load	Maximum Output Load	Ripple	Noise
1	+5V	+5 - 4%	1.5 A	20.0A	50 mV	100mV
2	-5V	+10 - 10%	0.0 A	0.5A	150 mV	200mV
3	+12V	+5 - 5%	0.2 A	8.0A	100 mV	200mV
4	-12V	+10 - 10%	0.0 A	0.5A	200 mV	200mV

1.10.2 350W Power Supply Specifications

Input Requirements

- Maximum waveform harmonic distortion shall be less than 5 percent. The power supply must operate above frequency with both 100~120/200~240 VRMS input voltage ranges.
- The power supply must operate over both voltage ranges with an outside switch.

Table 1-13 350W Power Supply Input Requirements

Input Frequency	Nominal Frequency 50 Hz 60 Hz	Frequency Variations 47 Hz ~ 53 Hz 57 Hz ~ 63 Hz
Input Voltage	Nominal Voltage 100 ~ 120 VRMS 200 ~ 240 VRMS	Variation Range 90 ~ 132 VRMS 180 ~ 264 VRMS
Input Current	Maximum Input Current 8.0A 4.0A	Measuring Range 90 ~ 132 VRMS 180 ~ 264 VRMS
Inrush Current	The power supply inrush current shall be less than the ratings of its critical components (including the fuse, rectifiers, and the surge-limiting device) for all conditions of line voltage.	
Efficiency	70% minimum (measuring at maximum load, applying nominal line)	

Output Requirements

- Ripple and noise bandwidth from DC to 20 MHz
- +12V should provide 17A surge current for the first 20 seconds after power on, and this regulation should be within +7% and -6%
- Total power consumption is 350 watts

Table 1-14 350W Power Supply Output Ratings (measured at output power connector)

Output	Nominal	Regulation	Minimum Output Load	Maximum Output Load	Ripple	Noise
1	+5V	+4 - 3%	5.0 A	43.0A	50 mV	100mV
2	-5V	+10 - 8%	0.0 A	1.0A	100 mV	200mV
3	+12V	+5 - 4%	----	10.0A	120 mV	200mV
4	-12V	+10 - 9%	----	1.0A	120 mV	200mV

1.11 Mechanical Specifications

1.11.1 ID3P Housing Specifications

Table 1-15 ID3P Housing Specifications

Main Board	Baby AT form factor
Housing Material	Plastic with metal shielding
Slots	8 full-size slots
Disk Drive Bays	3.5-inch: 1 External Disk Drive 5.25-inch: 3 External Disk Drives 3.5-inch: 2 Internal Disk Drives(1" Height)
Power Supply	200W PS/2 SPS
Dimension	155 mm (H) x 417 mm (D) x 432 mm (W)
Net Weight	5.5 kg
Color/Paint	Units are delivered in specified MCS colors. Paint samples are supplied to the vendor as required.
Metal Finish	All metal surfaces are plated, or with equivalent treatments.
Maximum Spacing	Spacing between adapter cards is 0.8 inches
Major Subassembly Support	Major subassemblies are rigidly held in place by frame components. Supports adequate clearances so that cards can be installed and removed without bending or forcing. All other components such as SPS and FDD can be assembled easily.
Circuit Cards Support	Circuit cards plugged into the system board are supported by a card edge connector, the card end bracket, and by a card edge guide supporting the card edge from the farthest end bracket (if the card conforms to the full length).

1.11.2 IDAB Housing Specifications

Table 1-16 IDAB Housing Specifications

Main Board	Baby AT form factor
Housing Material	Metal
Slots	8 full-size slots
Disk Drive Bays	3.5-inch: 2 External Disk Drives 5.25-inch: 3 External Disk Drives 3.5-inch: 2 Internal Disk Drives(1" Height)
Power Supply	200W PS/2 SPS
Dimension	400 mm (H) x 454 mm (D) x 190 mm (W)
Net Weight	7 kg
Color/Paint	Units are delivered in specified MCS colors. Paint samples are supplied to the vendor as required.
Metal Finish	All metal surfaces are plated, or with equivalent treatments.
Maximum Spacing	Spacing between adapter cards is 0.8 inches
Major Subassembly Support	Major subassemblies are rigidly held in place by frame components. Supports adequate clearances so that cards can be installed and removed without bending or forcing. All other components such as SPS and FDD can be assembled easily.
Circuit Cards Support	Circuit cards plugged into the system board are supported by a card edge connector, the card end bracket, and by a card edge guide supporting the card edge from the farthest end bracket (if the card conforms to the full length).

1.11.3 IDU Housing Specifications

Table 1-17 IDU Housing Specifications

Main Board	Baby AT form factor
Housing Material	Metal
Slots	11 full-size slots
Disk Drive Bays	3.5-inch: 1 External Disk Drive 5.25-inch: 3 External Disk Drives 3.5-inch: 8 Internal Disk Drives(1.6" Height)
Power Supply	200W PS/2 SPS or 350W L-type AT SPS
Dimension	590 mm (H) x 592 mm (D) x 180 mm (W)
Net Weight	17.5 kg
Color/Paint	Units are delivered in specified MCS colors. Paint samples are supplied to the vendor as required.
Metal Finish	All metal surfaces are plated, or with equivalent treatments.
Maximum Spacing	Spacing between adapter cards is 0.8 inches
Major Subassembly Support	Major subassemblies are rigidly held in place by frame components. Supports adequate clearances so that cards can be installed and removed without bending or forcing. All other components such as SPS and FDD can be assembled easily.
Circuit Cards Support	Circuit cards plugged into the system board are supported by a card edge connector, the card end bracket, and by a card edge guide supporting the card edge from the farthest end bracket (if the card conforms to the full length).